UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,774	03/30/2004	David K. Parker	02453.0033.NPUS00	8909

27194 7590 08/03/2009
HOWREY LLP-CA
C/O IP DOCKETING DEPARTMENT
2941 FAIRVIEW PARK DRIVE, SUITE 200
FALLS CHURCH, VA 22042-2924

EXAMINER	
AHMED, SALMAN	

ART UNIT	PAPER NUMBER
2419	

MAIL DATE	DELIVERY MODE
08/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,774	PARKER ET AL.	
	Examiner	Art Unit	
	SALMAN AHMED	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/28/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,24 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-22, 24, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okagawa et al. (US PAT PUB 2007/0291754, hereinafter Okagawa) in view of Hung et al. (US PAT 6530010, hereinafter Hung).

In regards to claims 1, 2, 4, 6, 8, 9 and 10 Okagawa teaches a processor readable medium (figure 3, element 50), which is physical, encoding a data structure for supporting one or more packet modification operations, the data structure comprising: a sequence of one or more commands, executable by a processor, implementing one or more packet modification operations and stored in a first memory area (paragraph 0062,

0063, the packet receiver 51.sub.a judges whether or not the received packet is the instruction information instructing it to update the function-mapping table 53. If yes, the packet receiver 51.sub.a transfers the packet to the interaction protocol transfer unit 51.sub.b. The interaction protocol transfer unit 51.sub.b, which is connected to the packet receiver 51.sub.a and the function-mapping control unit 52, transfers the packet (instruction information) from the packet receiver 51.sub.a to the function-mapping control unit 52); and a burst of one or more data or mask items, stored in a second memory area distinct from the first, for use by the processor in executing the one or more commands (paragraph 0085, The function-mapping table 53, which is connected to the function-mapping control unit 52 and the packet switch 56, is a first memory configured to store a packet ID (terminal ID) associated with a function unit 57.sub.1 to 57.sub.z of the control function executed on the packet (function ID) and a parameter required to execute the control function (various information element). As shown in FIG. 5, the configuration of the function-mapping table 53 is same as the configuration of the function-mapping cache table 51.sub.e); wherein at least one command in the sequence implements a packet modification operation that uses at least one of the one or more data or mask items to modify a packet (paragraphs 0123, 0124, 0130, In step 903, the function-mapping control unit 52 in the router device 50 updates the function-mapping table 53 in accordance with the instruction information which is received via the control signal network 2, or via the packet communications network 1 and the circuit interface 51. In step 904, the function-mapping unit 52 transmits information for updating the function-mapping cache table 51.sub.e (cache information) to the circuit

interfaces 51.sub.1 to 51.sub.n, and transmits information for updating the function-mapping cache table 57.sub.d (cache information) to the function units 57.sub.1 to 57.sub.z. In step 905, the function-mapping cache tables 51.sub.e in the circuit interfaces 51 are updated in accordance with the information, and the function-mapping cache tables 57.sub.d in the function units 57 are also updated in accordance with the information. According to the packet communications system of this embodiment, the function-mapping control unit 52 (manager) can update the function-mapping table 53 (first memory) in accordance with the instruction information received from the network manager 30, and the packet switch 56 (internal transfer) can transfer the received packet to the function unit 57 (executer) associated with the packet in the function-mapping table 53 (first memory), thus enabling the construction of the packet communications network 1 independently of the various network controls).

Okagawa does not explicitly teach using pointers to access memories.

Hung in the same or similar field of endeavor teaches data memory 145 and coefficient memory 147 may be written to in 128 bit words. This write operation is controlled by digital signal processor core 110 or direct memory access circuit 120 which, through the use of operand pointers in the commands, manage the two memory blocks (column 14, lines 64-67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Okagawa's system/method with the steps of using pointers to access memories as suggested by Hung. The motivation is that because a single copy of the common information can be maintained, and each of the replicated

copies can merely contain a pointer to this common information, substantial savings are achieved with respect to memory allocation and resources. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

In regards to claims 11, 12, 14, 16, 18, 20, 21 and 22 Okagawa teaches a method of performing one or more packet modification operations on a packet associated with a data structure link, the method comprising: retrieving from a memory a data structure corresponding to the data structure link, the data structure comprising a first pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area (paragraph 0062, 0063, the packet receiver 51.sub.a judges whether or not the received packet is the instruction information instructing it to update the function-mapping table 53. If yes, the packet receiver 51.sub.a transfers the packet to the interaction protocol transfer unit 51.sub.b. The interaction protocol transfer unit 51.sub.b, which is connected to the packet receiver 51.sub.a and the function-mapping control unit 52, transfers the packet (instruction information) from the packet receiver 51.sub.a to the function-mapping control unit 52), and a second pointer to a burst of one or more data or mask items, stored in a second memory area distinct from the first, for use by the processor in executing the one or more commands (paragraph 0085, The function-mapping table 53, which is connected to the function-mapping control unit 52 and the packet switch 56, is a first memory configured to store a packet ID (terminal ID)

associated with a function unit 57.sub.1 to 57.sub.z of the control function executed on the packet (function ID) and a parameter required to execute the control function (various information element). As shown in FIG. 5, the configuration of the function-mapping table 53 is same as the configuration of the function-mapping cache table 51.sub.e); retrieving from the first memory area the one or more commands; retrieving from the second memory area the one or more data or mask items; and executing the one or more commands by the processor, thereby performing one or more packet modification operations on the packet; wherein at least one of the one or more commands retrieved from the first memory area implements a packet modification operation that uses at least one of the one or more data or mask items to modify the packet (paragraphs 0123, 0124, 0130, In step 903, the function-mapping control unit 52 in the router device 50 updates the function-mapping table 53 in accordance with the instruction information which is received via the control signal network 2, or via the packet communications network 1 and the circuit interface 51. In step 904, the function-mapping unit 52 transmits information for updating the function-mapping cache table 51.sub.e (cache information) to the circuit interfaces 51.sub.1 to 51.sub.n, and transmits information for updating the function-mapping cache table 57.sub.d (cache information) to the function units 57.sub.1 to 57.sub.z. In step 905, the function-mapping cache tables 51.sub.e in the circuit interfaces 51 are updated in accordance with the information, and the function-mapping cache tables 57.sub.d in the function units 57 are also updated in accordance with the information. According to the packet communications system of this embodiment, the function-mapping control unit 52

(manager) can update the function-mapping table 53 (first memory) in accordance with the instruction information received from the network manager 30, and the packet switch 56 (internal transfer) can transfer the received packet to the function unit 57 (executer) associated with the packet in the function-mapping table 53 (first memory), thus enabling the construction of the packet communications network 1 independently of the various network controls).

Okagawa does not explicitly teach using pointers to access memories.

Hung in the same or similar field of endeavor teaches data memory 145 and coefficient memory 147 may be written to in 128 bit words. This write operation is controlled by digital signal processor core 110 or direct memory access circuit 120 which, through the use of operand pointers in the commands, manage the two memory blocks (column 14, lines 64-67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Okagawa's system/method with the steps of using pointers to access memories as suggested by Hung. The motivation is that because a single copy of the common information can be maintained, and each of the replicated copies can merely contain a pointer to this common information, substantial savings are achieved with respect to memory allocation and resources. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

In regards to claims 24 and 28 Okagawa teaches a memory storing a data structure comprising a first pointer to a sequence of one or more commands implementing one or more packet modification operations and stored in a first memory area (paragraph 0062, 0063, the packet receiver 51.sub.a judges whether or not the received packet is the instruction information instructing it to update the function-mapping table 53. If yes, the packet receiver 51.sub.a transfers the packet to the interaction protocol transfer unit 51.sub.b. The interaction protocol transfer unit 51.sub.b, which is connected to the packet receiver 51.sub.a and the function-mapping control unit 52, transfers the packet (instruction information) from the packet receiver 51.sub.a to the function-mapping control unit 52); and a second pointer to a burst of one or more data or mask items, stored in a second memory area distinct from the first, for use in the one or more packet modification operations (paragraph 0085, The function-mapping table 53, which is connected to the function-mapping control unit 52 and the packet switch 56, is a first memory configured to store a packet ID (terminal ID) associated with a function unit 57.sub.1 to 57.sub.z of the control function executed on the packet (function ID) and a parameter required to execute the control function (various information element). As shown in FIG. 5, the configuration of the function-mapping table 53 is same as the configuration of the function-mapping cache table 51.sub.e); and a processor configured to retrieve and execute the one or more commands pointed to by the first pointer; wherein at least one of the one or more commands implements a packet modification operation that uses at least one of the one or more data or mask items to modify a packet (paragraphs 0123, 0124, 0130, In step

903, the function-mapping control unit 52 in the router device 50 updates the function-mapping table 53 in accordance with the instruction information which is received via the control signal network 2, or via the packet communications network 1 and the circuit interface 51. In step 904, the function-mapping unit 52 transmits information for updating the function-mapping cache table 51.sub.e (cache information) to the circuit interfaces 51.sub.1 to 51.sub.n, and transmits information for updating the function-mapping cache table 57.sub.d (cache information) to the function units 57.sub.1 to 57.sub.z. In step 905, the function-mapping cache tables 51.sub.e in the circuit interfaces 51 are updated in accordance with the information, and the function-mapping cache tables 57.sub.d in the function units 57 are also updated in accordance with the information. According to the packet communications system of this embodiment, the function-mapping control unit 52 (manager) can update the function-mapping table 53 (first memory) in accordance with the instruction information received from the network manager 30, and the packet switch 56 (internal transfer) can transfer the received packet to the function unit 57 (executer) associated with the packet in the function-mapping table 53 (first memory), thus enabling the construction of the packet communications network 1 independently of the various network controls).

Okagawa does not explicitly teach using pointers to access memories.

Hung in the same or similar field of endeavor teaches data memory 145 and coefficient memory 147 may be written to in 128 bit words. This write operation is controlled by digital signal processor core 110 or direct memory access circuit 120

which, through the use of operand pointers in the commands, manage the two memory blocks (column 14, lines 64-67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Okagawa's system/method with the steps of using pointers to access memories as suggested by Hung. The motivation is that because a single copy of the common information can be maintained, and each of the replicated copies can merely contain a pointer to this common information, substantial savings are achieved with respect to memory allocation and resources. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

In regards to claims 3, 15 and 29, Okagawa and Hung do not explicitly teach first memory and second memory are located in the same memory. It would have been obvious i.e. "Obvious to try" – choosing from a finite number of identified, predictable solutions, to one having ordinary skill in the art at the time the invention was made to modify Okagawa and Hung's system/method with the steps of first memory and second memory being located in the same memory depending on system resources, system specification, network requirement, design choice etc. to implement an efficient system,

In regards to claims 5 and 17 Okagawa teaches one or more data or mask items are stored in packet format (figure 5).

In regards to claims 7 and 19, Okagawa and Hung do not explicitly teach first memory and second memory are located in a memory implemented off chip in relation

to te processor. It would have been obvious i.e. ”Obvious to try” – choosing from a finite number of identified, predictable solutions, to one having ordinary skill in the art at the time the invention was made to modify Okagawa and Hung’s system/method with the steps of first memory and second memory are located in a memory implemented off chip in relation to te processor depending on system resources, system specification, network requirement, design choice etc. to implement an efficient system,

4. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okagawa et al. (US PAT PUB 2007/0291754, hereinafter Okagawa) and Hung et al. (US PAT 6530010, hereinafter Hung) in view of Corby, Jr. et al. (US PAT 5524258, hereinafter Corby).

In regards to claim 30, Okagawa and Hung teach the one or more commands and all the limitations of claim 24, but do not explicitly teach a pipeline processor core configured to retrieve the one or more commands in a first stage, and execute the one or more commands in one or more subsequent stages.

Corby in the same or similar field of endeavor teaches a real-time data processing system employs a control computer which defines a pre-processing arrangement of data channels to speed processing, and an arrangement of output data channels to provide a desired output format. The data channels are samples and arranged into a data packet which is passed to an array of digital signal processors (DSPs) arranged in a series of stages, with at least one DSP per stage. A front-end DSP receives the data packet and appends a control field having commands addressed

to specific DSPs to the data packet along with adding a monitor field. The DSPs monitor the control field for commands addressed to it and then executes those. The status of the operation is written in the monitor field and the data packet is passed to DSPs of the next stage for `pipelined` processing. DSPs of the last stage collect the process portions of the data packet, assemble them according to the desired output format and pass on the completed data packet. The system control computer may monitor the monitor field of any data packet and determine the health of each DSP (abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Okagawa and Hung's system/method with the steps of a pipeline processor core configured to retrieve the one or more commands in a first stage, and execute the one or more commands in one or more subsequent stages as suggested by Corby. The motivation is that (as suggested by Corby lines 45-55, paragraph 1) a particularly useful way of arranging the many processors is to organize them as cascaded groups of processors, with each group forming a stage operating within the same time period. The outputs of a given stage form the inputs to the succeeding stage. The total processing task is decomposed into a finite set of sequential operations. This is called pipelining. These tasks are distributed over the stages of processor array; thus implementing an efficient processing system. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

Response to Arguments

1. Applicant’s arguments, see the Remarks sections, filed 6/23/2009, 6/24/2009 and 7/28/2009, with respect to the rejections of the claims have been fully considered and are moot in view of new ground of rejections presented in this office action.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SALMAN AHMED whose telephone number is (571)272-8307. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571)272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Salman Ahmed/

Examiner, Art Unit 2419